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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,315	10/31/2003	Yoshinori Shizuno	OHG 141	9863

23995 7590 09/11/2006

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EXAMINER	
ARORA, AJAY	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,315	SHIZUNO, YOSHINORI	
	Examiner	Art Unit	
	Ajay K. Arora	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/29/06*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *2-9 and 11-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/31/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/31/03; 10/27/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Embodiment 1 of Figures 1-3, on which read claims 1 and 10, in the reply filed on 8/29/2006 is acknowledged.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa (US 4,418,284), hereinafter Ogawa in view of Hashimoto (US 6,333,565), hereinafter Hashimoto.

Regarding claim 1, Ogawa (refer to Figure 3) teaches a semiconductor device which is packaged at substantially identical outer dimensions to the outer dimensions of a first semiconductor chip (15), comprising: first pads (6) provided on a main surface of said first semiconductor chip; a light-receiving element (Col. 4, line 33-35) portion (3) provided on said main surface of said first semiconductor chip such that a light-receiving surface (3) thereof is exposed; a light-transmitting portion (7) provided so as to cover

the light-receiving surface (3) of said light-receiving element portion for transmitting incoming light to said light-receiving element portion, a wiring layer (wiring part of layer 5 that connects to pads 6) which is electrically connected to said first pads (6).

However, Ogawa does not teach that the wiring layer "extends from said first pads over said main surface of said first semiconductor chip; and external terminals which are provided in a position opposing said wiring layer and electrically connected to said first pads via said wiring layer". Hashimoto (refer to Figure 1), which also discloses a semiconductor device which is packaged at substantially identical outer dimensions to the outer dimensions of a first semiconductor chip, teaches that a wiring layer (18/22) extends from first pads (14) over a main surface (surface with pads 14) of a first semiconductor chip (12); and external terminals (26) which are provided in a position opposing said wiring layer (18/22) and electrically connected to first pads (14) via the wiring layer (18/22). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Ogawa so that the wiring layer extends from said first pads over said main surface of said first semiconductor chip; and external terminals which are provided in a position opposing said wiring layer and electrically connected to said first pads via said wiring layer. The ordinary artisan would have been motivated to modify Ogawa for at least the purpose of creating a wafer scale package (WSP) by adding the interconnects and associated structure to the pads of the invention of Ogawa.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa in view of Hashimoto, and further in view of Lanford (US 5,959,358), hereinafter Lanford.

Regarding claim 10, Ogawa teaches substantially the claimed structure but does not teach that the device further comprises "post portions provided between said wiring layer and said external terminals; and a sealing layer provided on said wiring layer and on the side surfaces of said post portions, wherein an oxidation film is formed on the side surface of said post portions". Hashimoto (refer to Figure 1) teaches a semiconductor device, wherein the device further comprises post portions (formed in hole 20a) provided between a wiring layer (18/22) and external terminals (26); and a sealing layer (20) provided on said wiring layer (18/22).

Lanford teaches copper interconnects or wiring for microelectronic devices, wherein an oxidation film is formed on side surfaces of the interconnects/wiring (Col. 4, lines 1-9). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Ogawa so that an oxidation film is formed on the side surface of said post portions. The ordinary artisan would have been motivated to modify Ogawa for at least the purpose of creating an inert protective layer that prevents further oxidation of the post portions (Col. 4, lines 1-9).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ajay K. Arora whose telephone number is (571) 272-8347. The examiner can normally be reached on Mon through Fri, 8am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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